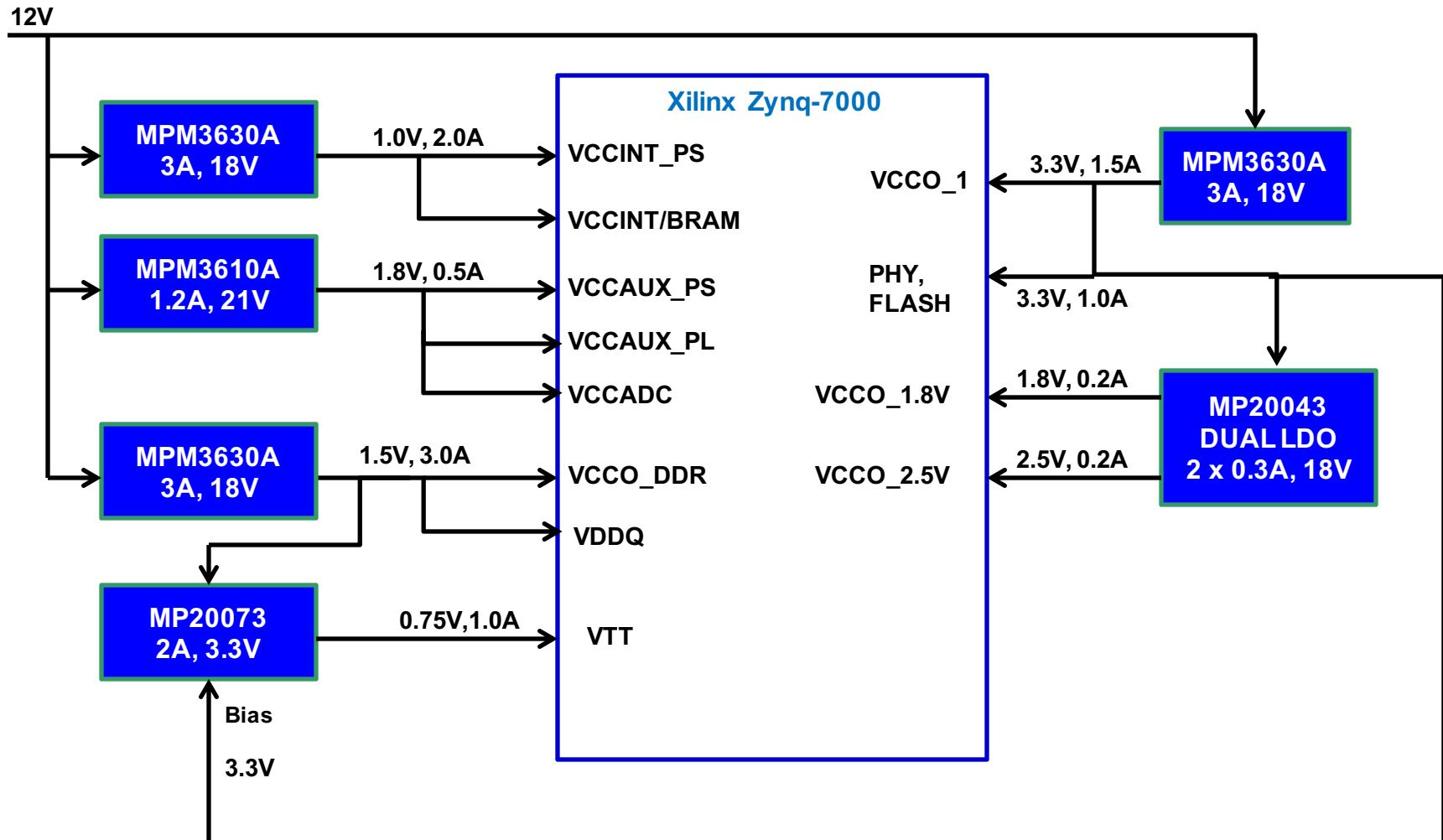
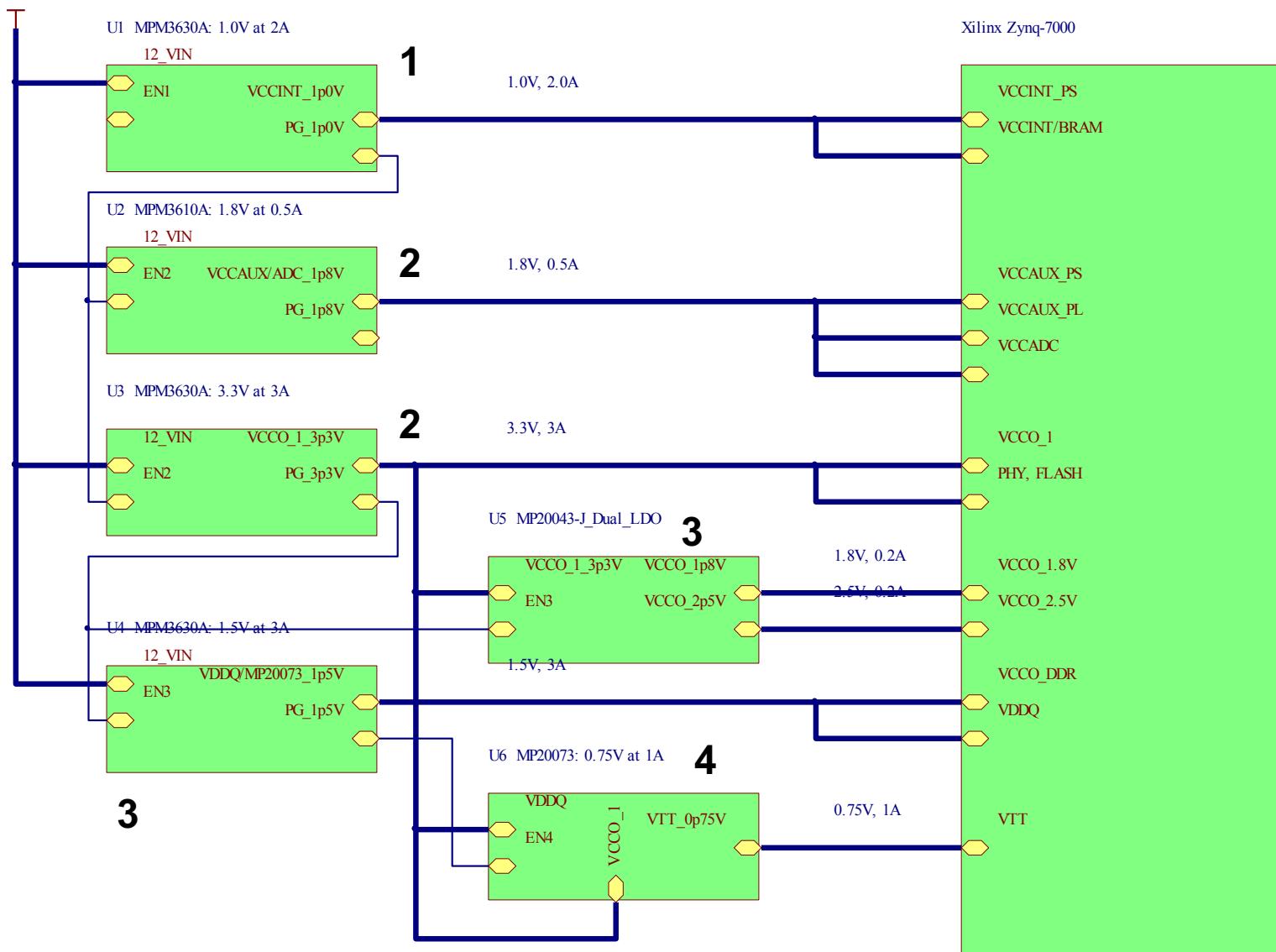


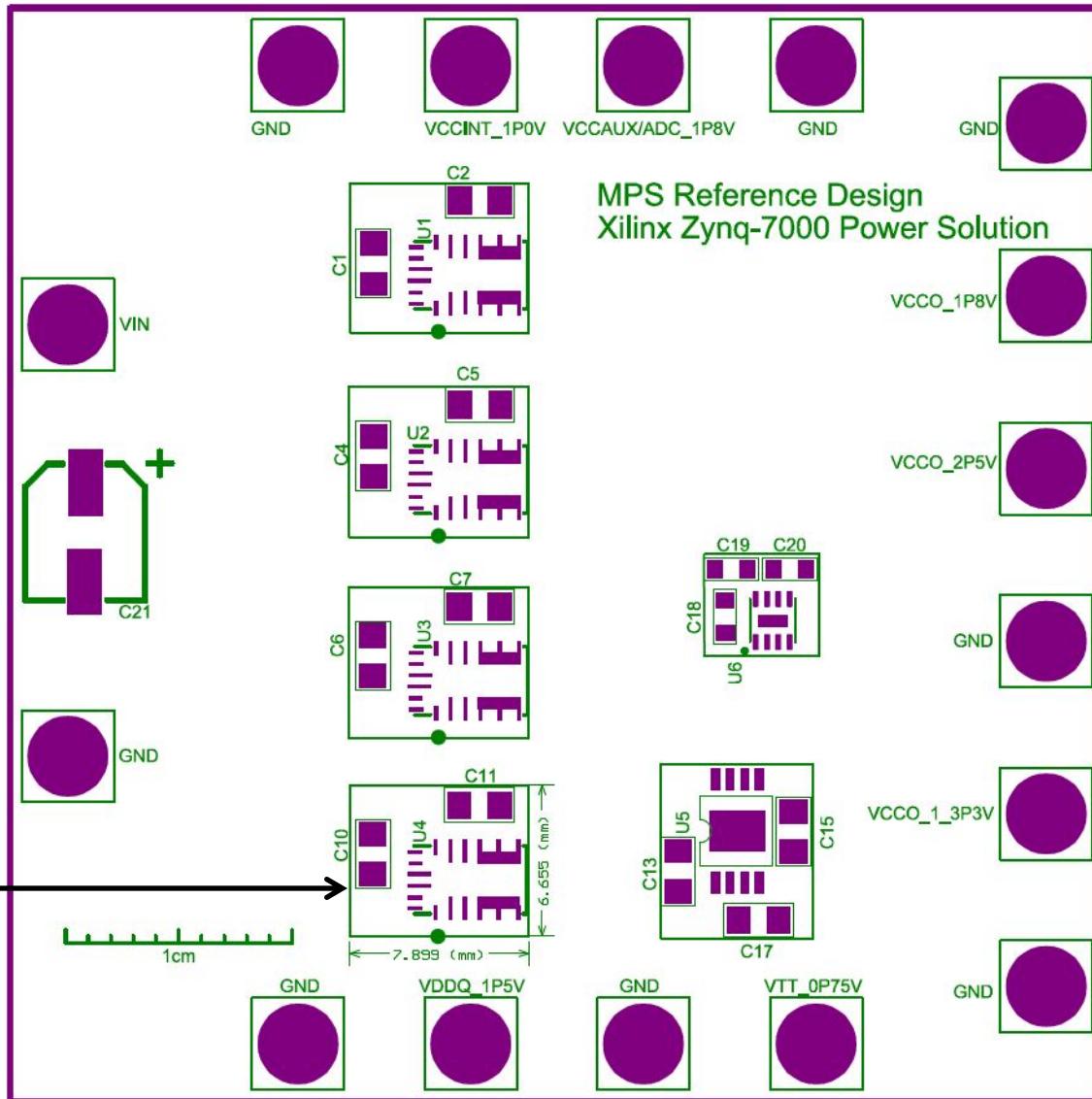


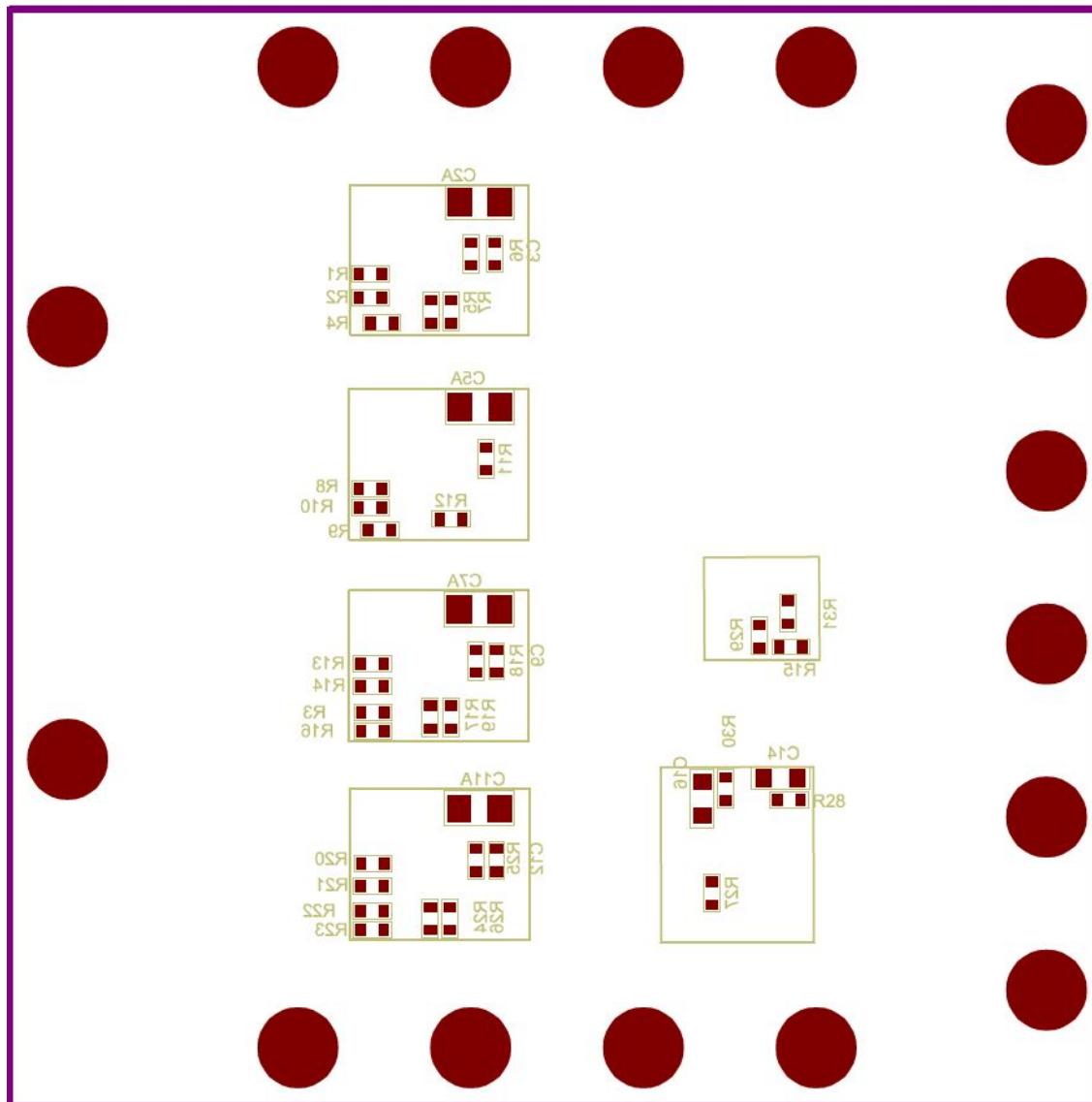
MPS Reference Design for Xilinx Zynq-7000

June 2016





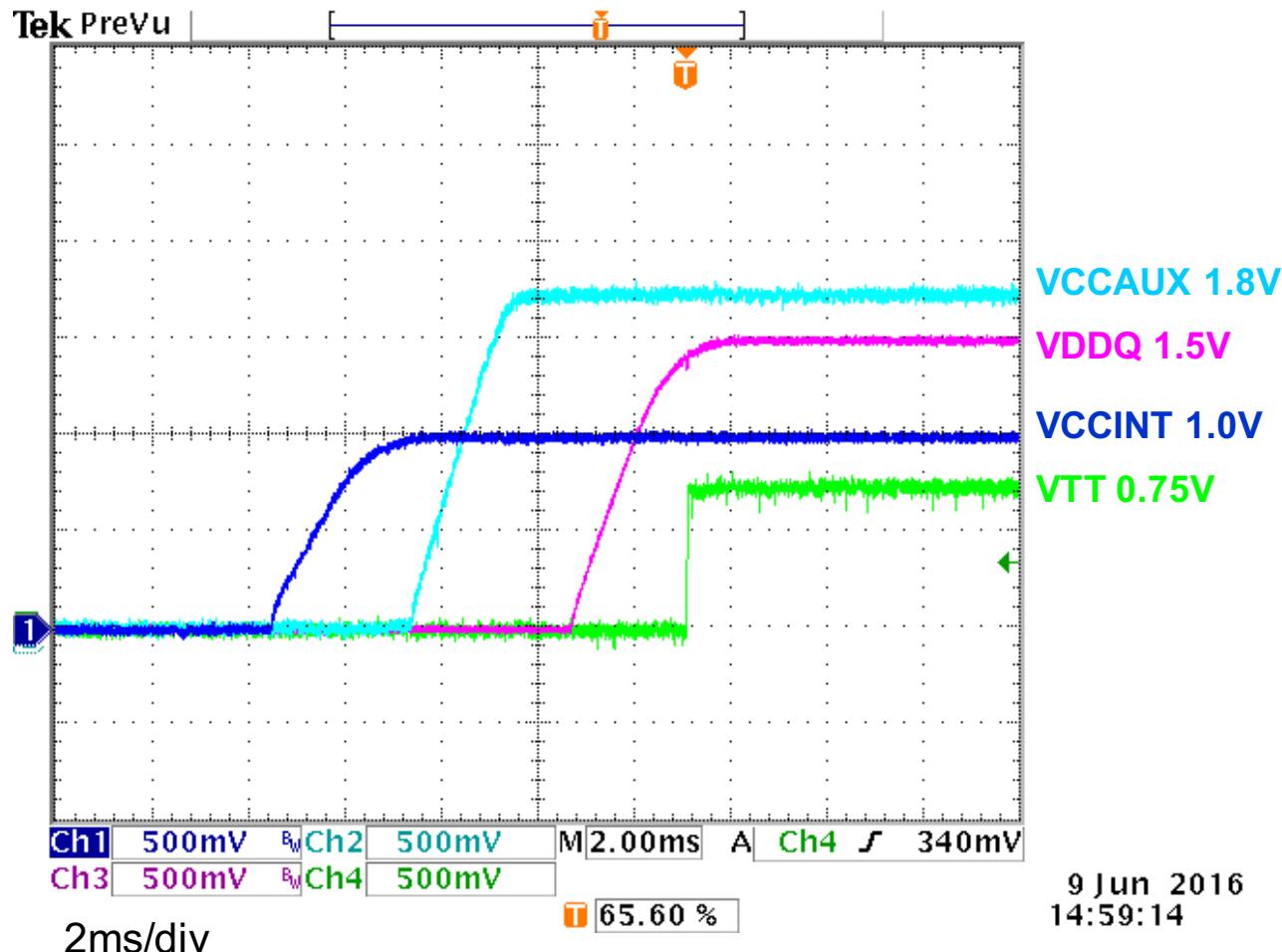




Item		Comment	Test Condition
Steady State	Efficiency	OK	3x MPM3630, MPM3610, MP20073, MP20043
	Output Ripple	OK	Full load/ No load
On/Off the part	Power on Sequence	OK	$V_{IN}=12V$, $I_{OUT}=0$ and full load
	Power off Sequence	DNS*	$V_{IN}=12V$, $I_{OUT}=0$ and full load

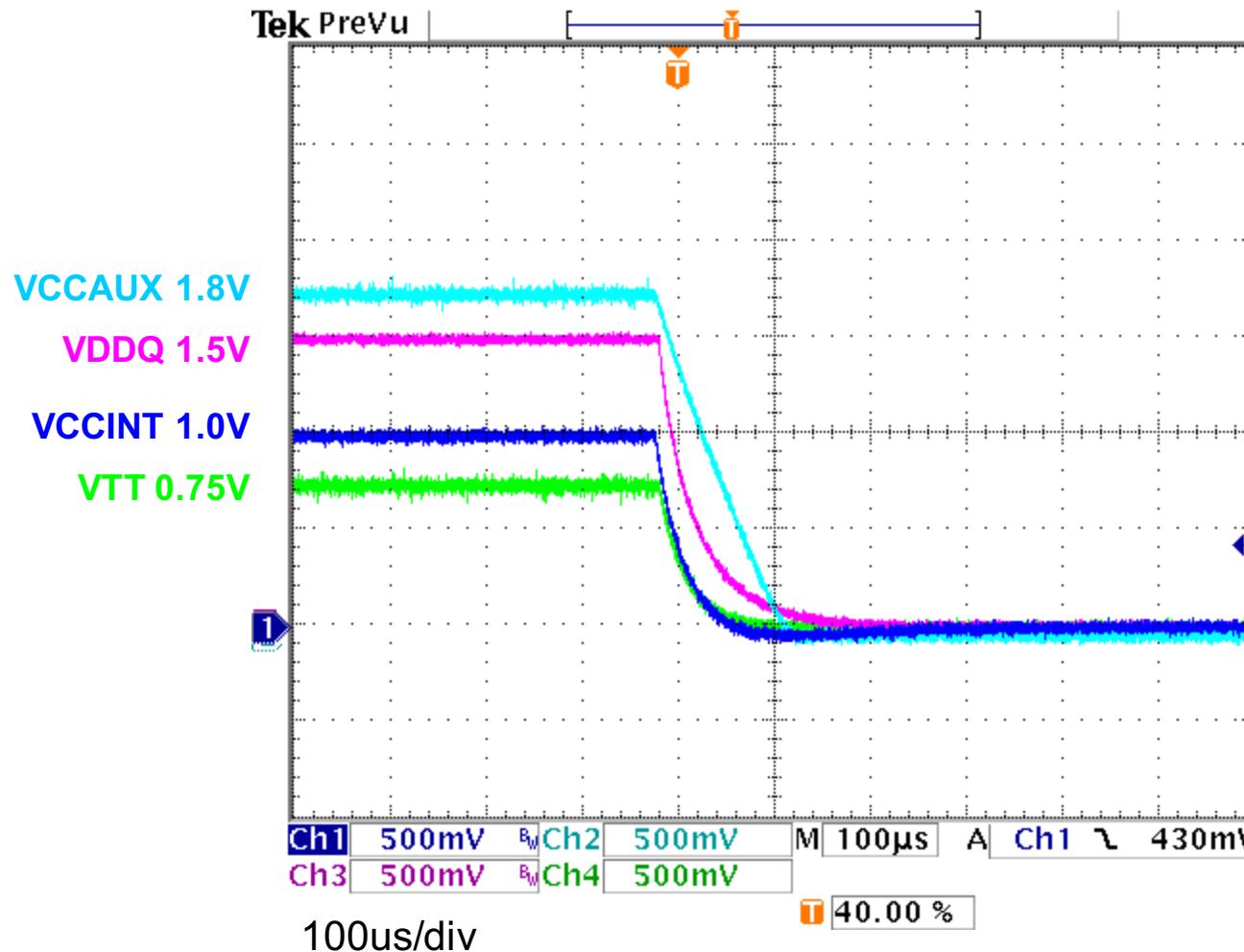
* **Does Not meet Spec.** Sequencing does not meet the requirements in the Ultrascale specification. External sequencing will be needed to provide the proper power down sequence, which is the complement of the powerup sequence. Contact MPS for Details.

$V_{IN}=12V$, full load in each rail

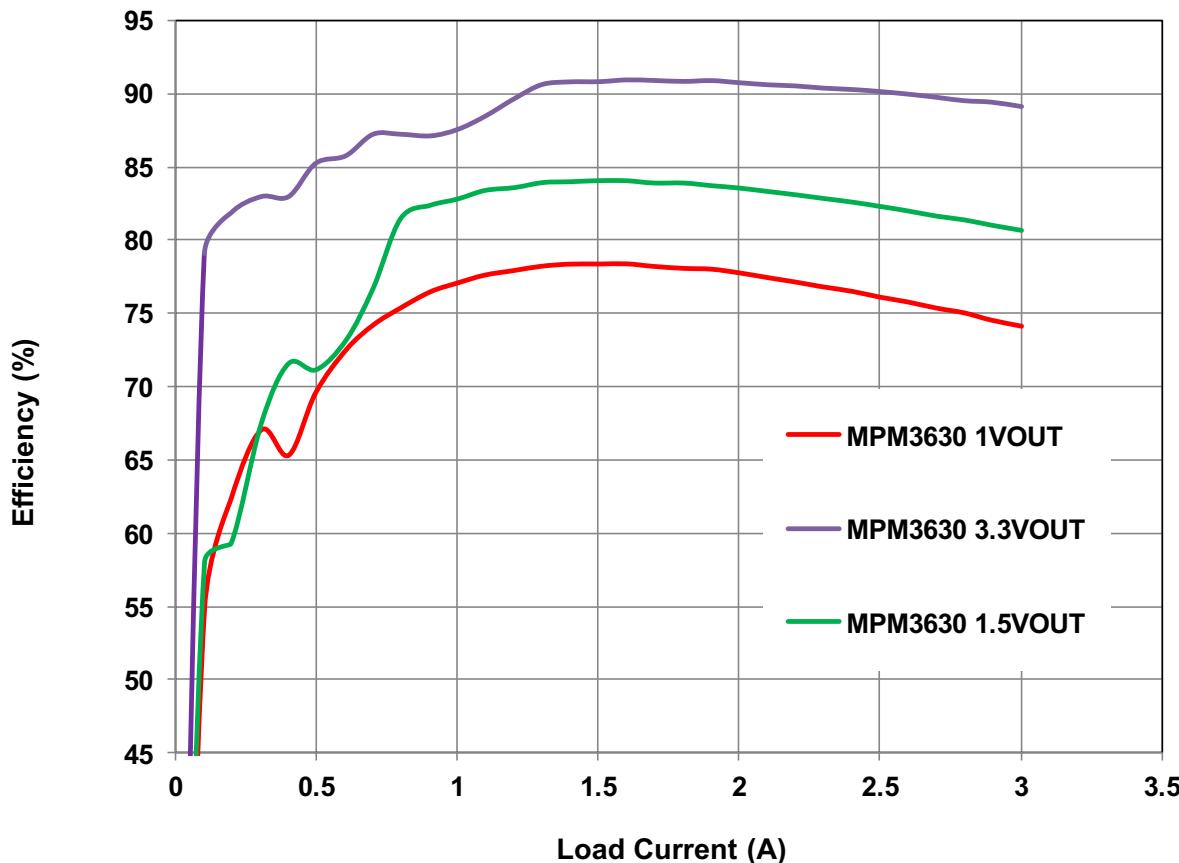


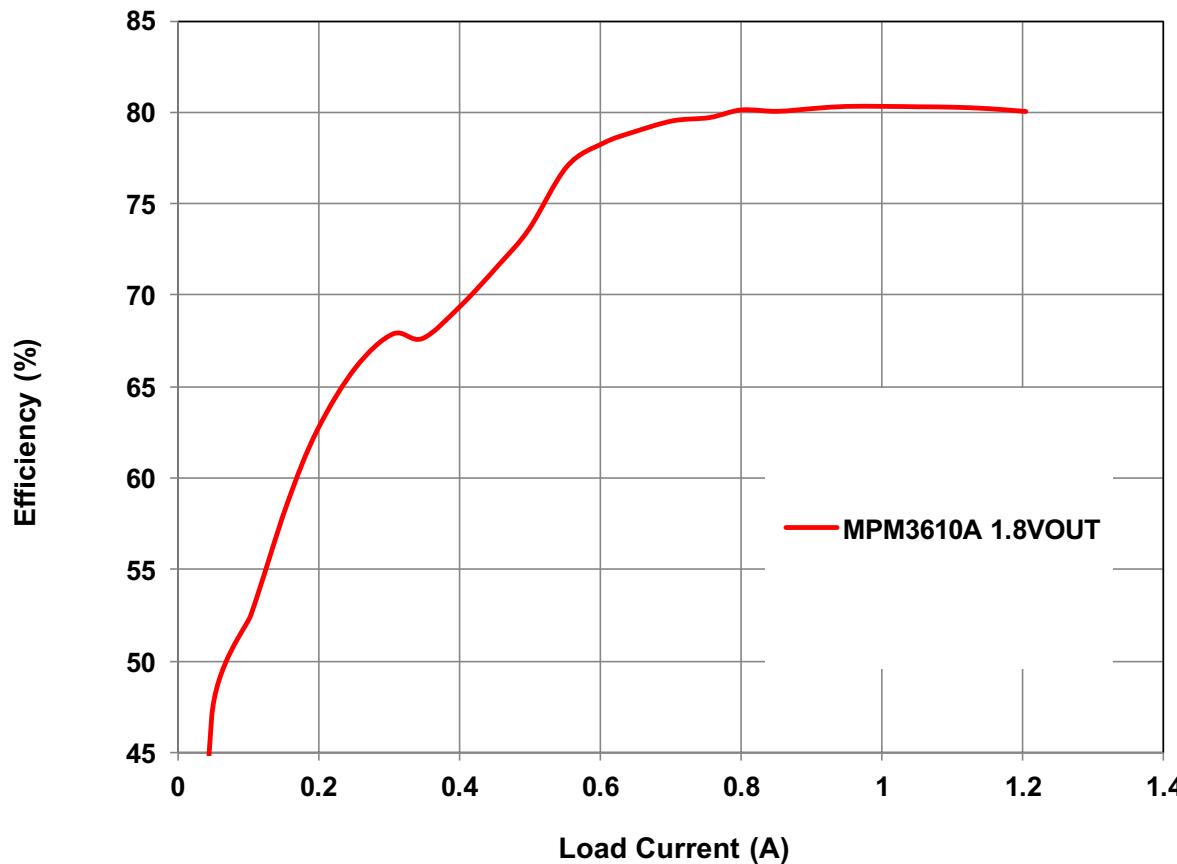
Power-down Through Enable Signal

V_{IN}=12V, full load in each rail

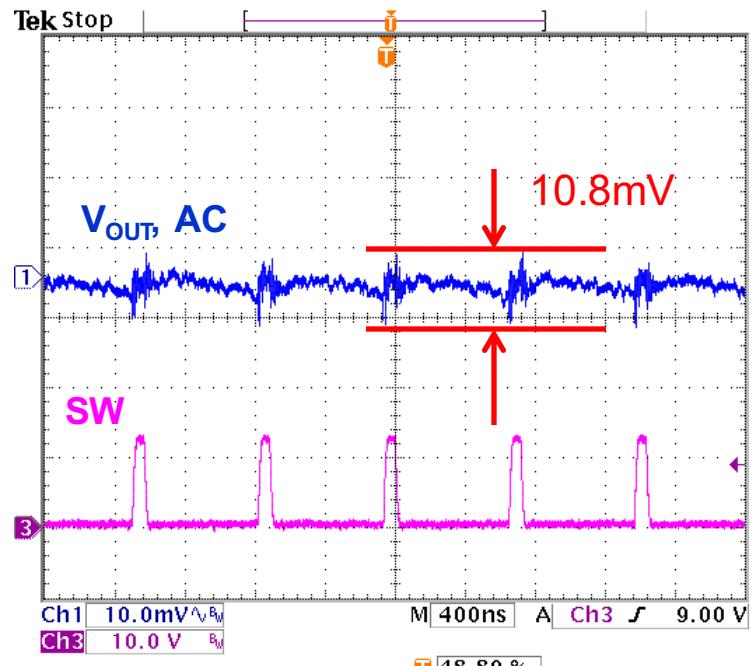


*Note that sequencing does not meet the requirements in the Ultrascale specification. External control is required to sequence the rails in the proper order. Contact MPS for Details.

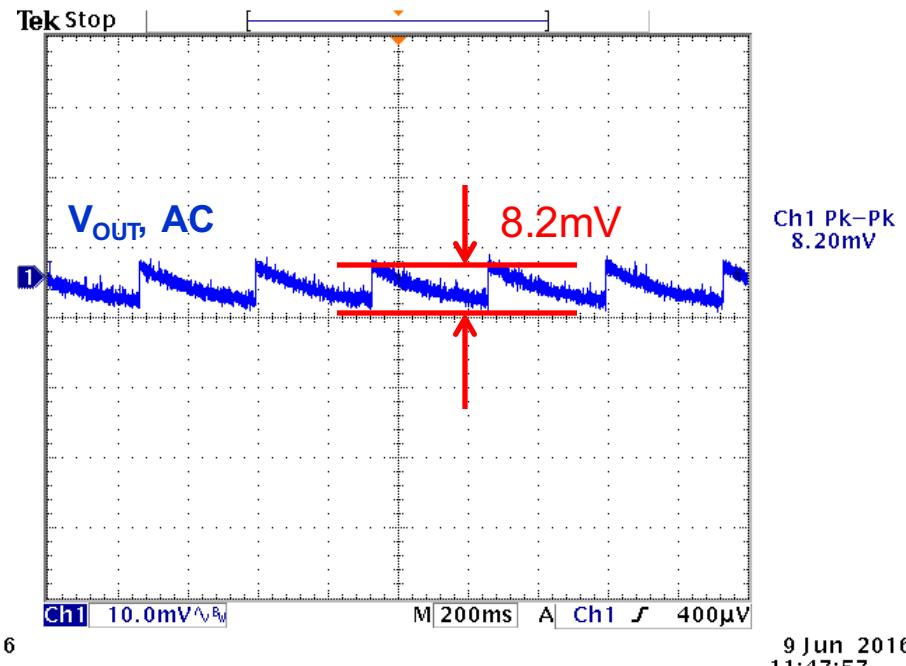
MPM3630 Efficiency, VIN=12V

MPM3610A Efficiency, VIN=12V

$V_{IN}=12V, V_{OUT}=1V, I_{OUT}=2A,$

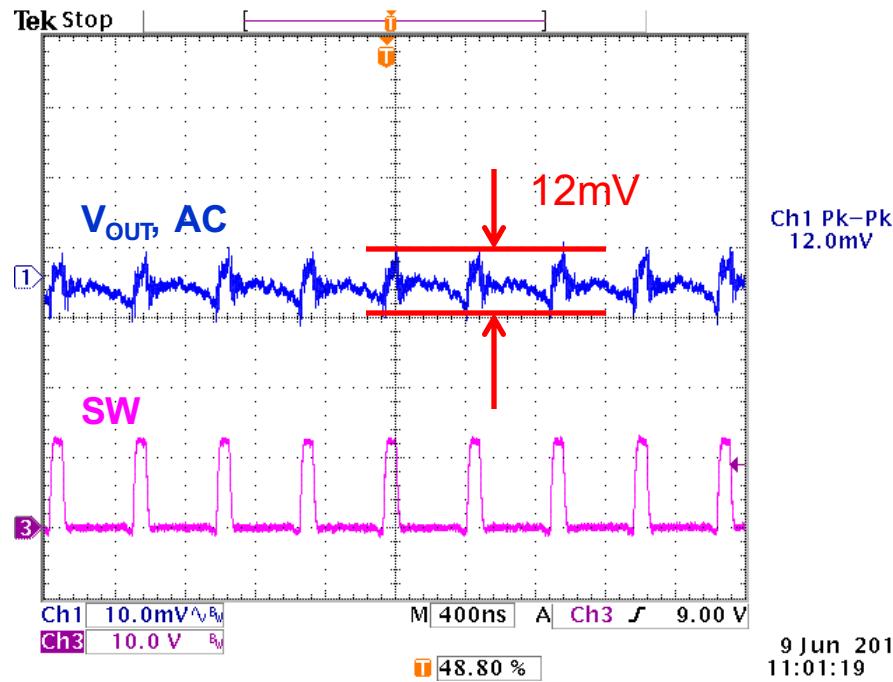


$V_{IN}=12V, V_{OUT}=1V, I_{OUT}=0A,$



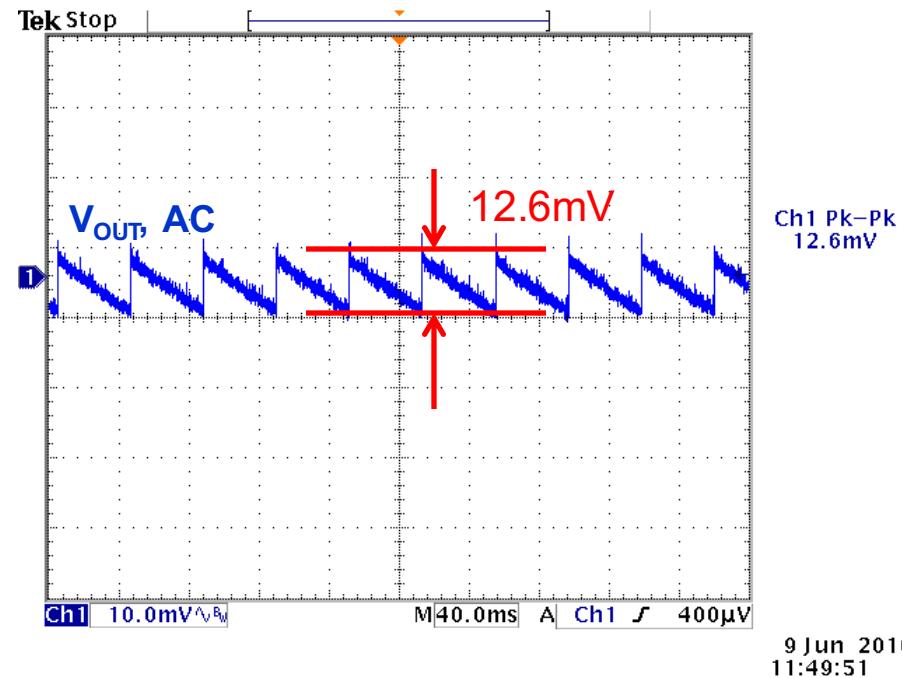
MPS® MPM3610A for VCCAUX 1.8V 0.5A Output Ripple

$V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0.5A,$



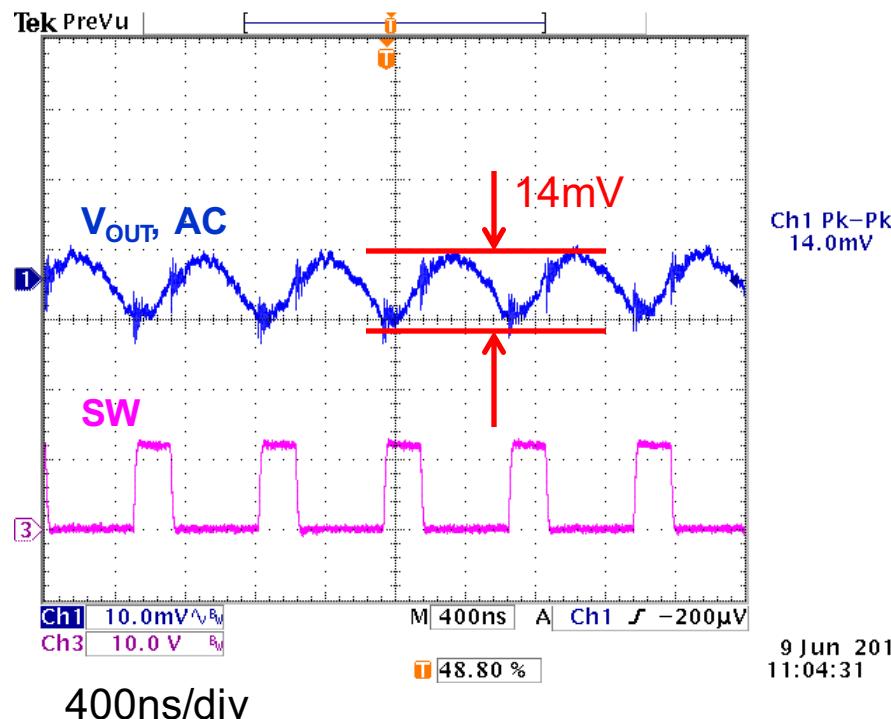
400ns/div

$V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0A,$

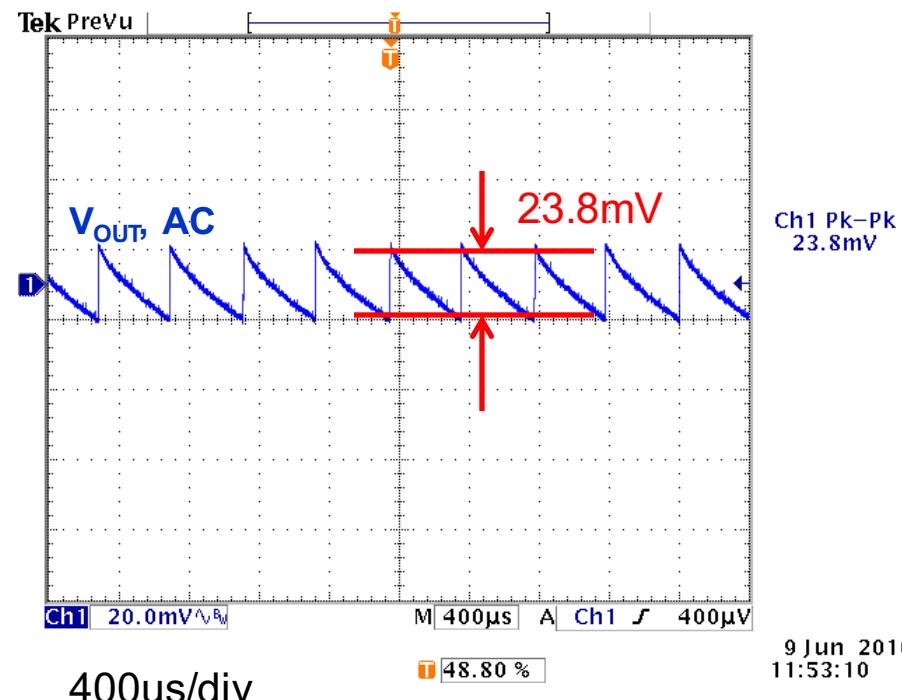


40ms/div

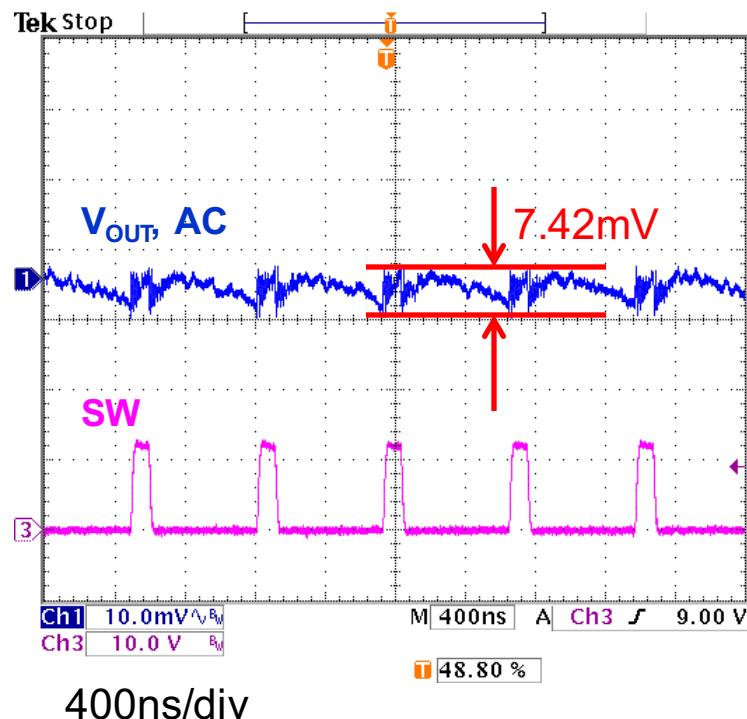
$V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A,$



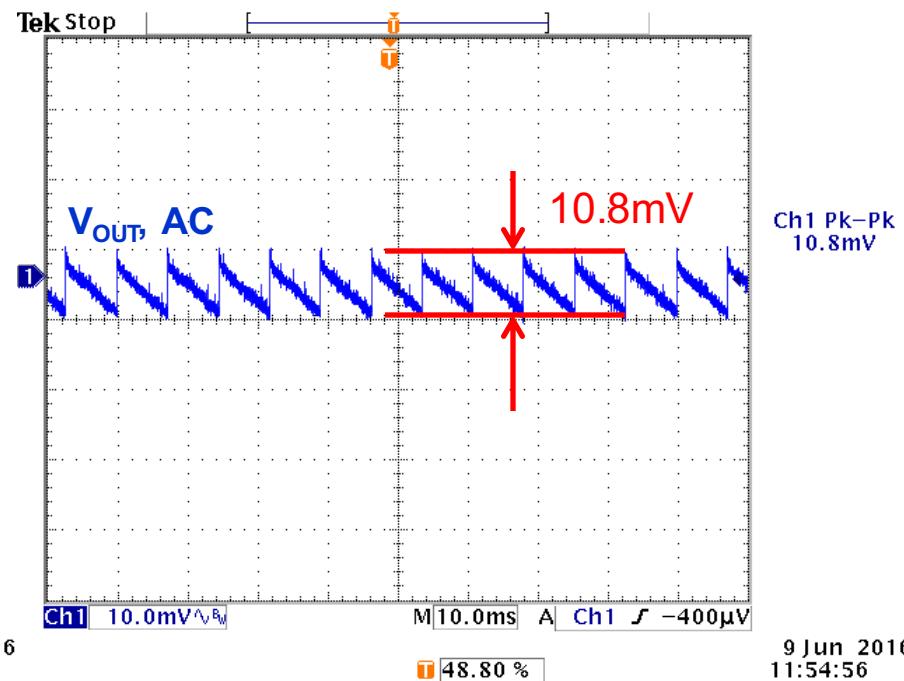
$V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A,$



$V_{IN}=12V$, $V_{OUT}=1.5V$, $I_{OUT}=3A$,



$V_{IN}=12V$, $V_{OUT}=1.5V$, $I_{OUT}=0A$,





Performance Summary

MPS Part #	Supply Rail	Solution Size (mm)	Efficiency	Voltage Ripple at Full Load
MPM3630	VCCINT 1V 2A	7x8	78.3%	10.8mV
MPM3610A	VCCAUX 1.8V 0.5A	7x8	75.2%	12mV
MPM3630	VCCO_1 3.3V 3A	7x8	89.2%	14mV
MPM3630	VDDQ 1.5V 3A	7x8	80.6%	7.42mV